

PTO 07-4881

CC=JA  
DATE=19900625  
KIND=PATENT  
PN=02164023

METHOD FOR FORMING SOI STRUCTURE AND SOI STRUCTURE  
[SOI Kozo No Keisei Hoho To SOI Kozo]

Hidekane Ogata et al.

UNITED STATES PATENT AND TRADEMARK OFFICE  
WASHINGTON, D.C.

JUNE 2007

TRANSLATED BY "SCHREIBER TRANSLATIONS INC."

PUBLICATION COUNTRY (10) : JAPAN

DOCUMENT NUMBER (11) : 02164023

DOCUMENT KIND (12) : PATENT

PUBLICATION DATE (43) : 19900625

APPLICATION NUMBER (21) : 63320924

APPLICATION DATE (22) : 19881219

INTERNATIONAL CLASSIFICATION (51) : H 01 L 21/205, 21/86

PRIORITY COUNTRY (33) :

PRIORITY NUMBER (31) :

PRIORITY DATE (32) :

INVENTOR(S) (72) : Hidekane Ogata et al.

APPLICANT(S) (71) : Sanyo Electric Co.,  
Ltd.

DESIGNATED CONTRACTING STATES (81) :

TITLE (54) : METHOD FOR FORMING SOI  
STRUCTURE AND SOI  
STRUCTURE

FOREIGN TITLE [54A] : SOI Kozo No Keisei  
Hoho To SOI Kozo

Specification

1. Title of the invention

Method for Forming SOI Structure and SOI Structure

2. Claims

1. A method for forming a SOI structure, characterized by consisting of a process for forming a single crystal semiconductor film on a single crystal insulating base; a process for making said single crystal semiconductor film porous; and a process for forming a single crystal semiconductor film on the porous single crystal semiconductor film.

2. The method for forming a SOI structure of Claim 1, characterized by the fact that the above-mentioned single crystal insulating base is a single crystal sapphire base; and the above-mentioned single crystal semiconductor film is a single crystal Si film.

3. A SOI structure, characterized by being formed of a single crystal semiconductor film formed via a porous single crystal semiconductor film on a single crystal insulating base.

---

<sup>1</sup> Numbers in the margin indicate pagination in the foreign text.

4. The SOI structure of Claim 3, characterized by the fact that the above-mentioned single crystal insulating base is a single crystal sapphire base; and the above-mentioned porous single crystal semiconductor film and the above-mentioned single crystal semiconductor film are single crystal Si films.

3. Detailed explanation of the invention

(Industrial application field)

The present invention pertains to a method for forming a SOI structure. In particular, the present invention pertains to a method for forming a single crystal Si film on a single crystal sapphire substrate.

(Prior art)

The structure in which a single crystal Si layer is formed on an insulating layer (also including an insulator substrate) is called a SOI (Silicon on Insulator) structure, and it is known that an element separation can be easily carried out in a narrow region and a high integration and a high speed can be realized in this structure. Then, compared with a conventional semiconductor integrated circuit (IC) in which elements are prepared on a Si substrate, since the characteristics can

be improved, this structure is actively researched and developed.

As one of the SOI structure, there is a structure in which a single crystal Si film is formed on a single crystal sapphire substrate. In this structure, a Si film is usually grown at a growth temperature of 900-1,000°C on a sapphire substrate by a CVD (Chemical Vapor Deposition) method.

However, since the thermal expansion coefficient is different between the sapphire substrate and the Si substrate (sapphire of  $9.5 \times 10^{-6}/^{\circ}\text{C}$ , Si is  $4.2 \times 10^{-6}/^{\circ}\text{C}$ ), a two-dimensional compressive stress is applied into the Si film at the stage where the substrate temperature is dropped to room temperature after the Si film growth. Since this compressive stress lowers the electron mobility of the Si film (see "Applied Physics," Vol. 49 (1980), p.110 published by the Society of Applied Physics), good characteristics cannot be obtained, so that there was an inconvenience in the formation of elements on the grown Si film.

For example, the compressive stress of the Si film (film thickness: 0.4 μm) formed on the sapphire substrate by the CVD method is about  $9.5 \times 10^9 \text{ dyn/cm}^2$ , and the Hall mobility of electrons at that time is only about 0.62 times

(SOI film with a carrier density of  $10^{10}$ - $10^{14}$  cm<sup>3</sup>) of the mobility of a bulk Si.

Also, even if the Si film on the sapphire substrate is grown at a growth temperature of 700°C by a molecular beam epitaxial (MBE) method, the compressive pressure of the Si film (film thickness: 0.1 μm) is about  $5 \times 10^9$  dyn/cm<sup>2</sup>, the compressive stress is not considerably decreased even by lowering the growth temperature of the Si film.

(Problems to be solved by the invention)

The present invention considers the above-mentioned points, and its purpose is to provide a SOI structure that does not have a large residual stress (compressive strength) of a single crystal Si film formed on a sapphire substrate and can obtain good characteristics by forming elements.

(Means to solve the problems)

The present invention is a method for forming a SOI structure characterized by consisting of a process for forming a single crystal Si film on a sapphire base, a process for making said single crystal Si film porous; and a process for forming a single crystal Si film on the porous single crystal Si film.

(Operation)

With the formation of the SOI structure by interposing the porous Si film between the single crystal Si film of the upper layer for preparing elements and the sapphire base, the porous Si film functions as a buffer material, and the compressive strength of the single crystal Si film of the upper layer is relaxed.

(Application example)

Figures 1A-C are illustrative diagrams showing the processes of an application example of the present invention. (1) is a single crystal sapphire base as a single crystal insulating base in which (1<sup>-</sup>012) plane (R plane) is a principal plane. Then, a single crystal Si film (2) is epitaxially grown at a growth temperature of 700°C, a growth rate of 10-20 Å/sec, and a film thickness of about 1,000 Å on the principal plane by a MBE method (Figure 1A).

Next, the substrate on which the single crystal Si film is growth is drawn out of the MBE device not shown in the figure, and an arsenic (8) is ion-implanted into the single crystal Si film (2). The ion implantation is carried out at an acceleration energy of 25 keV and the amount of dose of  $1 \times 10^{15} \text{ cm}^{-2}$ , so that the single crystal film (2) is changed to a p type. Furthermore, the above-

mentioned substrate is immersed into 50% fluoric acid as an electrolytic solution, and the single crystal Si film (2) on the substrate is anodized at a current density of 5 mA/cm<sup>3</sup>. With the anodization, the single crystal Si film (2) is made porous at a rate of 70 Å/sec (Figure 1B).

As the porous single crystal Si, for example, it is known that if the single crystal Si is made porous by the anodization like this application example, a single crystal Si structure having many pores with a radius of 20-100 Å is obtained and its density is 40-70%. For this reason, the porous single crystal Si has an elasticity, compared with a perfect crystal Si.

After making the single crystal Si film (2) porous (the porous single crystal Si film is called (2')). Again, a substrate is set in a MBE apparatus not shown in the figure. Then, a SOI structure is formed on the porous single crystal Si film (2') under the conditions of a growth temperature of 700°C and a growth rate of 10-20 Å/sec similar to the above-mentioned ones by an epitaxial growth at a film thickness of 3,000 Å (Figure 1C).

The internal stress (compressive stress) in the single crystal Si film in the SOI structure formed in this manner was measured by a laser Raman spectroscopy. As a result, it was about  $2.5 \times 10^7$  dyn/cm<sup>2</sup>. Compared with the internal

stress (compressive stress) in the single crystal Si film with the conventional SOI structure in which the single crystal Si film being an active layer for forming elements is directly formed on the sapphire substrate, a large/3 internal stress decrease is realized.

The reason for this is that the porous Si film (2') relaxes the internal stress being generated by the difference in the thermal expansion coefficient between the sapphire substrate (1) and the single crystal Si film (3), on which elements are formed, by its elasticity.

Then, with the decrease of the internal stress, the Hall mobility of the electrons of the single crystal Si film (3) is about 0.88 times of that of a bulk Si and is improved, compared with the prior art, so that the characteristics of elements being formed on the single crystal Si film (3) can be improved.

(Effects of the invention)

As seen from the above explanation, according to the present invention, since a porous Si film is formed on a sapphire substrate and a single crystal Si film for forming elements is grown on the Si film, the residual stress (internal stress) being generated from the difference in the thermal expansion coefficient between the sapphire substrate and the Si is relaxed. Then, the Hall mobility

of electrons of the single crystal Si film is improved, so that the characteristics of elements being formed on said single crystal Si film can be improved.

#### 4. Brief description of the figures

Figures 1A-C are illustrative diagram showing the processes of an application example of the present invention.

- (1) Sapphire substrate (single crystal insulating base)
- (2), (3) Single crystal Si films (single crystal semiconductor films)
- (2') Porous Si film (porous single crystal semiconductor film)

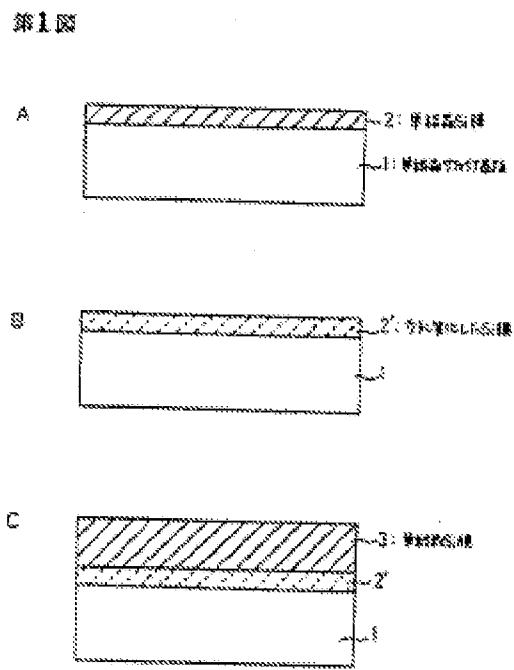


Figure 1:

- 1 Single crystal insulating base
- 2 Single crystal Si film
- 2' Porous Si film
- 3 Single crystal Si film